Tanta University
Faculty of Engineering
Computer and Control Dep.
Second Year

Second Term – Final Exam
Subject: Computer Architecture
Allowed Time: 3 Hours
Date: June 15, 2011

# Answer the following 2 questions and assume any missing data:

## Question 1: [Computer Arithmetic]                                      45 Marks

1. Design 8-bit carry look-ahead adder with minimum gate delay that adds $x_{0-7}$ to $y_{0-7}$ then produces $s_{0-7}$ and $c_8$. After that compute the delay of $s_7$ and $c_8$ in milliseconds (msec) assuming that the delay of each OR gate is 3 msec, each AND gate 5 msec, and each NOT gate is 2 msec.

(15 Marks)

2. Multiply $0110100 \times 11110110$ using:
   a.  Booth Algorithm                          b.  Bit pairing recording of multipliers

(10 Marks)

3. Draw the hardware circuit that can perform integer division, and then write the algorithms for both the restoring and non-restoring division. Show how the second algorithm is driven from the first then use the non-restoring algorithm to divide: $1100\ 0001 \div 1010$.

(10 Marks)

4. Use 32-bit IEEE standard for floating point numbers to represent the following numbers in binary:

   a.  $(+ 23.125)_{10}$                         c.  $\infty$

   b.  $(- 141.25)_{10}$                         d.  $(- 0.001100 \times 2^{-126})_2$

(10 Marks)

## Question 2: [Input/Output Organization]                               45 Marks

1. Design a centralized bus arbitration system that applies daisy chain between 4 I/O devices assuming that all control devices are active high. Then draw the time sequence of signals that transfer the bus mastership to device number 2.

(10 Marks)

2. Draw and explain the handshake control signals of data transfer over asynchronous bus during an output operation.

(10 Marks)

3. Discuss the operation of the Direct Memory Access showing the functions of its interface registers.

(10 Marks)

4. Design an interface circuit between the processor and a printer assuming that the computer has 32-bit address bus, 16-bit data bus, status flag bit is transferred over line $D_{15}$ of the data bus, and address line $A_{31}$ is used as control signal, then design the logic circuit that can generate the status flag bit properly.

(15 Marks)

Good Luck                                                    *Dr. Tarek El.Ahmady El.Tobely*